A production Chemical Mechanical Planarization (CMP) tool in a research environment

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• Since 1987
• Operated by KTH and RISE
• Part of Myfab
• 1 300 m² cleanroom ISO 5-6
• 1 500 m² other labs
• About 250 Users
• Yearly turnaround 5.5 MEuro
• Open access policy
• 50/50 academic/commercial
• Education, research, development and small scale production
• Process lines: Si (MEMS and CMOS); SiC; InP and GaAs
• ISO 9001 and ISO 14001 certified management and environmental system
CMP Process Motivation

• Polishing removing surface roughness

• Planarization enabling multi layer structures

• Technologies:
  • Monolithic integration: materials and devices
  • Wafer bonding
  • Dielectric layer planarization
  • Metal interconnection
  • Epitaxial regrowth
  • Layer polishing

CMP Process Motivation
- Enabling 3D integration

• Planarization enables integration:
  • Heterogeneous 3D integration
  • Close packing and extreme miniaturization
  • Complex systems

• Applications
  • CMOS
  • Power Electronics
  • Optoelectronics
  • MEMS & System-on-chip
CMP Process - basics

- Platen with polishing pad:
  - Polyurethane based
  - Hardness, density, structure

- Slurry
  - Chemical action
  - Mechanical grinding (particle size ~ 20 - 100 nm)

- Wafer carrier
  - Down force (up to 340 kg)
  - Pressure distribution for uniformity

- Pad conditioner:
  - Diamond coated disc
  - Revitalization of the polishing pad
  - Pad longevity and process reproducibility

Preston formula for CMP removal rate ($RR$):

- $RR \propto P, v$
  - $P$ – polishing pressure
  - $v$ – relative velocity between pad and wafer

CMP Tool: IPEC 472

• Specification: flexibility & high performance
  • 2 polishing tables: primary and buffing
  • Removable table tops for fast process switching
  • 2 slurry lines per table
  • Wafer diameters: 50, 75, 100, 150, (and 200) mm
  • Cassette-to-cassette handling for 100 and 150 mm
  • Temperature control of polishing platens
  • State of the art uniformity with Titan™ wafer carrier
  • Materials: Si/SiGe; SiO₂; SiC; InP; GaAs

• Peripherals:
  • External 110 l slurry tank with stirring
  • Wet cabinet for pad storage
  • Megasonic bath for post CMP cleaning
  • Water circulation system (retrofit)
CMP tool installation requirements

Dimensions:
• 200 x 170 cm
• Height: 235 cm

Weight:
• 3410 kg

Media:
• DI water: 20 l/min
• CDA: 170 SLM
• Exhaust: 600 m³/hr
Titan™ Wafer carrier
For state-of-the-art uniformity

- Wafer sizes
  - Separate heads for 100 & 150 mm (200 mm available)
  - Insert ring in the 150 mm head for 50 and 75 mm

- 3 pressure zones for uniformity:
  - RR - Retainer Ring
  - IT - Inner Tube
  - MM – Membrane pressure
  - Vacuum for wafer loading

Process control PECVD SiO₂ process
In a multi-user environment

- Polishing rate over months
- Surface roughness
- Wafer to wafer non-uniformity
- Within wafer non-uniformity

<table>
<thead>
<tr>
<th>RR</th>
<th>WIWNU</th>
<th>WTWNU</th>
<th>Rs</th>
</tr>
</thead>
<tbody>
<tr>
<td>510 nm/min</td>
<td>3 %</td>
<td>2 %</td>
<td>0.7 nm</td>
</tr>
<tr>
<td>230 nm/min</td>
<td>2 %</td>
<td>1 %</td>
<td>0.8 nm</td>
</tr>
<tr>
<td>80 nm/min</td>
<td>5 %</td>
<td>5 %</td>
<td>0.3 nm</td>
</tr>
</tbody>
</table>

Statistical Process Control

st. dev. ≈ 18 %
Wafer handling and Process
Wet handling

- Post CMP wet handling of wafers
  - Wet receiver cassette
  - Wet transfer boxes to post CMP cleaning

- Post CMP cleaning procedure:
  - DI water in megasonic bath
  - Standard Clean 1 & 2
  - Rinse-Dryer

- Wet handling of pads
  - Wet storage cabinet
  - Platen DI-water flushed

**Total DI-water consumption:**
- Up to 20 l/min at process
- 3 l/min at stand-by
- Saving goal: 1 l/min
Example 1: CMP a key enabler for monolithic 3D integration

- Multi layer transistor circuits
  - 1\textsuperscript{st} tier: Si based transistors
  - 2\textsuperscript{nd} tier: Ge based transistors

- Complex fabrication process by epitaxial growth and wafer bonding, enabled by CMP.
Ex 1: Transfer of SiGe layer on patterned substrate

(a) SiO₂ (400 nm)
(b) CMP removed ~ 1 µm
(c) Strain relaxed SiGe ~ 3 µm
(d) After removal of Si substrate and Ge buffer layer

Strain relaxed SiGe ~ 3µm
Ex 1a: Reduce roughness of SiGe strain relaxed buffer

Epitaxial SiGe layer before CMP step
Spikes is ten’s of nm

after CMP step
RMS surface roughness ≈ 0.9 nm

SiO$_2$ 250 nm
PECVD

Si$_{0.5}$Ge$_{0.5}$ < 20 nm
Epitaxy

Strain relaxed SiGe ~ 3μm
Si wafer
Ex 1b: Reduce roughness of PECVD SiO₂

As deposited
AFM roughness = 3.7 nm

Post CMP
Roughness = 0.8 nm

Height of the slurry particles:
40-100 nm

Post CMP: H₂O megasonic clean for 30 min
Ex 1c: Planarization of PECVD SiO$_2$ on metals

Before planarization

600 nm removal

1200 nm removal

Step height ~ 670 nm

Step height ~ 70 nm

Step height ~ 3 nm
Example 2: Planarization of GaAs epitaxy on Si Substrate

**BEFORE CMP**

Rq(20\(\mu\)m) = 85 nm

**AFTER 360 nm**

Rq(20\(\mu\)m) = 3.1 nm
Rq(4\(\mu\)m) = 0.8 nm

\[ RR = 14\pm2 \text{ nm/min} \]
Example 3: Process for full 3DSiC© structure

3DSiC© structures for buried grid high blocking voltage applications

**Two step process**

1. Primary slurry
   - High removal rate: 7 µm/h (Si face)
2. Final slurry
   - Removal rate: 1 µm/h (Si face)
   - Low surface roughness: 0.5 nm \( R_{\text{rms}} \)

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Courtesy to Ascatron AB

Part of myfab

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Example 4: Planarization of thick SiC epitaxial layer surface

For >30 µm thick SiC epilayers surface degrades due to step-bunching and defects

Typical surface after 260 µm n-epi

Nomarski microscope image
AFM

Surface after CMP

Rms = 138nm
Rms = 0.5nm

Courtesy to Ascatron AB
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